

Claim 43 has features that are similar to the other independent claims in question, and will serve as a model for comparison to U.S. Patent No. 6,628,142.

The features of U.S. Patent No. 6,628,142, as recited in independent claim 1, include an enabling signal, an input signal and an inhibit signal, all presented to an input buffer having a component that inhibits semiconductor breakdown. The enabling signal is a feature not found in the claims of the present application, and is described in the detailed description of U.S. Patent No. 6,628,142 as protecting the circuit from ESD events occurring when the semiconductor device is not in operation, for example when a Flash chip is being handled, or when there is a high voltage test mode in the memory. Applicant respectfully submits that the enabling signal is a claimed feature of U.S. Patent No. 6,628,142 that is not found in the present application, and the presence of this feature results in system operations that are different from the present device and have different operational outcomes in similar circumstances.

One feature of the present claims not found in U.S. Patent No. 6,628,142 is the bias circuit that acts in tandem with the pass transistor under the control of the inhibit signal, to place the internal signal node at a predetermined voltage whenever the pass transistor has interrupted the input signal to the internal signal node. The claims of U.S. Patent No. 6,628,142 do not recite this feature. Applicant respectfully submits that this is another example of how the operation of the present device results in different outcomes under similar circumstance as compared to U.S. Patent No. 6,628,142.

There are other features of U.S. Patent No. 6,628,142 that are not found in the present claims including the first through fourth clamping circuits to hold the input signal at various levels, and the first through fourth predetermined voltage levels, and the multiple thin gate oxide transistor, but Applicant respectfully submits that the two specific examples given above of the differences in the arrangement and the differences in the resulting operations are sufficient by themselves to show that the present claims are not a case of double patenting as compared to claims 1-43 of U.S. Patent No. 6,628,142. In view of the above discussion, Applicant respectfully requests that the double patenting rejection be withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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August 16, 2004

By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 16 day of August, 2004.

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Signature

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